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0-1	International Application No.	
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0-3	Name of receiving Office and "PCT International Application"	
0-4	Form PCT/RO/101 PCT Request	
0-4-1	Prepared Using	PCT-SAFE Version 3.50 (Build 0002.162)
0-5	Petition The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
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0-7	Applicant's or agent's file reference	SH-21710-PCT
I	Title of Invention	METHOD OF GENERATING PARITY INFORMATION USING LOW DENSITY PARITY CHECK
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V	DESIGNATIONS	
V-1	The filing of this request constitutes under Rule 4.9(a), the designation of all Contracting States bound by the PCT on the international filing date, for the grant of every kind of protection available and, where applicable, for the grant of both regional and national patents.	
V-2	Item V-2 may be used to exclude (irrevocably) the designations concerned in order to avoid the ceasing of the effect, under the national law, of an earlier national application from which priority is claimed. As to the consequences of such national law provisions in these and certain other States, see Designations in PCT-SAFE Help.	KR
VI-1	Priority claim of earlier national application	
VI-1-1	Filing date	28 November 2003 (28.11.2003)
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VI-1-3	Country	KR
VII-1	International Searching Authority Chosen	Korean Intellectual Property Office (ISA/KR)

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VIII	Declarations	Number of declarations	
VIII-1	Declaration as to the identity of the inventor	-	
VIII-2	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	-	
VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	-	
VIII-4	Declaration of inventorship (only for the purposes of the designation of the United States of America)	-	
VIII-5	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty	-	
IX	Check list	number of sheets	electronic file(s) attached
IX-1	Request (including declaration sheets)	5	✓
IX-2	Description	9	✓
IX-3	Claims	3	✓
IX-4	Abstract	1	✓
IX-5	Drawings	6	✓
IX-7	TOTAL	24	
	Accompanying Items	paper document(s) attached	electronic file(s) attached
IX-8	Fee calculation sheet	-	✓
IX-11	Copy of general power of attorney	-	reference no. 6-1-2004-0000213-65
IX-17	PCT-SAFE physical media	-	-
IX-19	Figure of the drawings which should accompany the abstract	3	
IX-20	Language of filing of the international application	English	
X-1	Signature of applicant, agent or common representative	(PKCS7 Digital Signature)	
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X-1-3	Capacity		

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10-1	Date of actual receipt of the purported international application	
10-2	Drawings:	
10-2-1	Received	
10-2-2	Not received	
10-3	Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application	
10-4	Date of timely receipt of the required corrections under PCT Article 11(2)	
10-5	International Searching Authority	ISA/KR
10-6	Transmittal of search copy delayed until search fee is paid	

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PCT REQUEST (ANNEX - FEE CALCULATION SHEET)

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(This sheet is not part of and does not count as a sheet of the international application)

0	For receiving Office use only		
0-1	International Application No.		
0-2	Date stamp of the receiving Office		
0-4	Form PCT/RO/101 (Annex)		
0-4-1	PCT Fee Calculation Sheet Prepared Using	PCT-SAFE Version 3.50 (Build 0002.162)	
0-9	Applicant's or agent's file reference	SH-21710-PCT	
2	Applicant	SAMSUNG ELECTRONICS CO., LTD.	
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12-1	Transmittal fee T	⇒	45000
12-2-1	Search fee S	⇒	225000
12-2-2	International search to be carried out by	KR	
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12-4	Remaining sheets	0	
12-5	Additional amount (X)	0	
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12-7	i1 + i2 = i	1329000	
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12-13	Total International filing fee (i-R) I	⇒	1044000
12-14	Fee for priority document		
	Number of priority documents requested	0	
12-15	Fee per document (X)	0	
12-16	Total priority document fee: P	⇒	
12-17	TOTAL FEES PAYABLE (T+S+I+P)	⇒	1314000
12-19	Mode of payment	cash	

Description

METHOD OF GENERATING PARITY INFORMATION USING LOW DENSITY PARITY CHECK

Technical Field

- [1] The present invention relates to a method of generating parity information, and more particularly, to a method of independently generating row parity information and column parity information in an encoding process using a low density parity check (LDPC) matrix.

Background Art

- [2] A low density parity check (LDPC) encoding and decoding method refers to an error correction encoding and decoding technology used in a wireless communication field and an optical recording/reproducing field. The LDPC encoding method was initially suggested by Gallager in 1962. However, since it was very difficult to manufacture a decoder at that time, the LDPC encoding method has been abandoned. Recently, the LDPC encoding method has been repropose by Mackey.
- [3] The LDPC encoding method includes a process of generating parity information using a parity check matrix. Here, most components of the parity check matrix are 0, and very sparse components of the parity check matrix are 1. The LDPC encoding method has an excellent error correction performance by performing repeatedly an encoding process using an adding/multiplying algorithm. For example, an irregular LDPC encoding process where the length of encoding language is 10^6 and an encoding rate is 1/2 has a performance closer to the Shannon limit, better than that of a turbo encoding process.
- [4] The LDPC encoding process is divided into a regular LDPC encoding process and an irregular LDPC encoding process. In the regular LDPC encoding process, the number of 1s included in a parity check matrix used for encoding and decoding is the same in every row and in every column. Otherwise, the LDPC encoding process is irregular.
- [5] The LDPC encoding process can be represented as shown in Equation 1.
- [6] [Equation 1]
- [7] $H \times C_e = 0$
- [8] where, H indicates a parity check matrix, 0 indicates a zero matrix, '×' indicates an XOR operation and a modular 2 operation, and C_e indicates a code word matrix which includes a number of code word vector. The code word vector includes an x-bit

message word x_1, x_2, \dots, x_x and p -bit parity information p_1, p_2, \dots, p_p .

- [9] The parity information p_1, p_2, \dots, p_p is generated so that the message word x_1, x_2, \dots, x_x satisfies Equation 1. That is, since a binary value of the message word to be coded among components of the parity check matrix H and matrix C_e is determined, parity information p_i ($i=1, 2, \dots, p$) can be determined using Equation 1.
- [10] A more detailed description of the LDPC encoding process is described in the article 'Good Error Correction Codes Based on Very Sparse Matrices' (D.J.MacKay, IEEE Trans. on Information Theory, vol. 45, no.2, pp.399-431, 1999).
- [11] In the LDPC encoding process, parity information is generated in every code word vector. That is, row parity information for decoding is generated. In a general block encoding process, the generation of column parity information is required for obtaining an excellent decoding performance. In a representative block encoding method such as the Reed-Solomon encoding method, column and row parity information are generated.
- [12] FIG. 1 illustrates a concept of generating row parity information in an LDPC encoding process. Referring to FIG. 1, A, B, C, D, ... indicate code word vectors, respectively, $a_1, a_2, \dots, b_1, b_2, \dots$ indicate message word bits included in the respective code word vectors, and P_A, P_B, P_C, \dots indicate column parity information generated in the respective code word vectors.
- [13] In a general block encoding process used for an optical disc system such as a DVD, one block size is 32 through 64 Kbytes. On the other hand, since a length of a general code word vector used for an LDPC encoding process is about 1 Kbytes, the number of columns in a block used for the LDPC encoding process is 32 through 64. When row parity information is generated, it is not efficient in the side of an error correction performance using the parity information to generate the parity information for only 32 through 64 bits. Therefore, when the row parity information is generated in the LDPC encoding process, it is general that the row parity information is generated by dealing with a plurality of rows together. FIG. 1 illustrates that a row encoding process of 4 code word vectors is performed by dealing with 2 rows together.
- [14] However, since the row encoding method sequentially extracts code word bits existing in code word vectors to be row encoded from a top position, errors are generated due to a correlation existing in the LDPC encoding process. Accordingly, it is impossible to generate independent parity information. That is, according to a method of selecting objects of the row parity information in one code word vector, row parity information may have a correlation with column parity information, and in this

case, when an error is generated in the column parity information, an error is also generated in the row parity information. Accordingly, the reliability of the row parity information is reduced.

Disclosure of Invention

Technical Solution

- [15] The present invention provides a method of generating row parity information without any correlation with generation of column parity information in an encoding process using a low density parity check (LDPC) matrix.

Advantageous Effects

- [16] By using a method of generating row parity information without any correlation with generation of column parity information in an encoding process using a low density parity check (LDPC) matrix, errors generated in the column parity information do not influence the row parity information.

Description of Drawings

- [17] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:
- [18] FIG. 1 illustrates generation of row parity information in an LDPC encoding process;
- [19] FIG. 2 is a flowchart of an LDPC encoding method according to an embodiment of the present invention;
- [20] FIG. 3 illustrates an arrangement of code word bits selected for generating row parity information in the LDPC encoding method according to an embodiment of the present invention;
- [21] FIG. 4 illustrates a correlation between a structure of a parity check matrix and code word bits;
- [22] FIG. 5 is a factor graph representing the parity check matrix of FIG. 4;
- [23] FIG. 6 illustrates a method of selecting correlated code word bits using a factor graph;
- [24] FIG. 7 illustrates a method of selecting a succeeding selectable code word bit when code word bit '3' is selected as a second code word bit in FIG. 6;
- [25] FIGS. 8 through 10 illustrates procedures of selecting residual code word bits when code word bit '2' is selected as a first code word bit in the parity check matrix of FIG. 4; and
- [26] FIG. 11 is a flowchart of a method of selecting code word bits for generating row

parity information using a factor graph.

Best Mode

- [27] According to an aspect of the present invention, there is provided an encoding method using a low density parity check (LDPC) matrix, the method comprising: generating code word vectors by generating column parity information using a parity check matrix and message information; selecting code word bits for generating row parity information among code word bits in the generated code word vectors; and generating the row parity information using the selected code word bits, wherein the selecting code word bits comprise: excluding code word bits related to the generation of other row parity information.
- [28] According to another aspect of the present invention, there is provided a method of selecting code word bits used for generating parity information in an information generating operation using an LDPC matrix, the method comprising: selecting a first code word bit; and selecting a second code word bit among residual code word bits except code word bits having a correlation with the first code word bit, wherein if the first code word bit is related to the generation of row parity information, and if, in a row number where a component corresponding to the first code word bit in the parity check matrix is 1, a component corresponding to the second code word bit in the row of the parity check matrix is 1, there is a correlation between the first and second code word bits.

Mode for Invention

- [29] Hereinafter, the present invention will now be described more fully with reference to the accompanying drawings, in which embodiments of the invention are shown.
- [30] FIG. 2 is a flowchart of an LDPC encoding method according to an embodiment of the present invention.
- [31] When message word bits are defined, code word vectors A, B, C, ... are generated by generating column parity information on the basis of Equation 1 described above. The column parity information is generated in a column encoding process in step 210. Code word bits to perform a row encoding process with respect to a code word vector are selected in step 220. Here, the selected code word bits must not have a correlation with a parity check matrix H. Code word bits to perform the row encoding process with respect to each of the other code word vectors are selected in step 230. The row encoding process is performed by generating row parity information as many as the number of rows according to a predetermined block size on the basis of the selected code word bits in step 240.

[32] FIG. 3 illustrates an arrangement of code word bits selected for generating row parity information in the LDPC encoding method according to an embodiment of the present invention. Referring to FIG. 3, code word vectors A, B, C, and D have code word bits $a_1, a_2, a_3, \dots, b_1, b_2, b_3, \dots$, respectively. Unlike the conventional method of FIG. 1, the code word bits selected by a row encoding method according to the present invention are not sequentially selected in the respective code word vectors. The code word bits a_1 and a_5 selected in the code word vector A are not correlated with each other. The present invention provides a method of selecting the non-correlated code word bits by selecting a certain code word bit and removing code word bits correlated with the certain code word bit.

[33] FIG. 4 illustrates a correlation between a structure of a parity check matrix and code word bits.

[34] When a binary value change of each code word bit in a code word vector causes a change in the same row parity information, the code word bits are correlated with each other. A method of seeking code word bits correlated with a specific code word bit from a structure of a parity check matrix will now be described.

[35] Column parity information P_A, P_B, \dots is generated using Equation 1 so that a result of multiplying (XOR operation and modular 2 operation) a parity check matrix H by respective code word vectors A, B, C, and D is a zero matrix. To generate the column parity information P_A , elements influencing the column parity information P_A in the parity check matrix H are all 1s existing in the parity check matrix H. However, when the column parity information P_A is generated, components including a specific component, for example, a_1 , of the code word vector A influence the generation of the column parity information P_A only when a component h_{jk} of the parity check matrix H multiplied by each component of the code word vector A is 1. It is shown in Equation 2.

[36] [Equation 2]

$$[37] \quad \text{mod } 2 [h_{11} a_1 + h_{12} a_2 + \dots h_{1n} a_n + h_{1n+1} P_{1A} + h_{1n+2} P_{2A} + \dots] = z_1$$

$$[38] \quad \text{mod } 2 [h_{21} b_1 + h_{22} b_2 + \dots h_{2n} b_n + h_{2n+1} P_{1B} + h_{2n+2} P_{2B} + \dots] = z_2$$

[39] ...

[40] where, h_{jk} indicates jth row -kth column components of the parity check matrix, a_1, a_2, \dots are components of the code word vector A, and P_{1A}, P_{2A}, \dots are column parity information generated with respect to the code word vector A.

[41] Therefore, when a component of the parity check matrix corresponding to a specific code word bit (a_1 in FIG. 4) is 1, if components (403, 404, and 405 in FIG. 4)

of the parity check matrix corresponding to other code word bits to be multiplied are 1, the other code word bits are correlated with the specific code word bit. That is, code word bits corresponding to locations where components in the same rows of the parity check matrix are 1 are correlated with each other.

[42] If it is assumed that the specific code word bit is a_1 in the parity check matrix of FIG. 4, components 401 and 402 corresponding to a_1 in the parity check matrix are 1.

[43] In a case of the component 401, that is, when the code word bit a_1 is multiplied by 1 in the first row and first column of the parity check matrix, components 404 and 405 are placed on locations where components in the row of the parity check matrix including the component 401 are 1. Therefore, code word bits a_4 and a_6 corresponding to the components 404 and 405 are correlated with the code word bit a_1 .

[44] In a case of the component 402, that is, when the code word bit a_1 is multiplied by 1 in the third row and first column of the parity check matrix, a component 403 is placed on a location where a component in the row of the parity check matrix including the component 402 is 1. Therefore, a code word bit a_2 corresponding to the component 403 is correlated with the code word bit a_1 .

[45] Accordingly, code word bits correlated with a_1 are a_2 , a_4 , and a_6 . That is, code word bits a_1 , a_2 , a_4 , and a_6 influence the generation of the column parity information P_A together.

[46] These correlated code word bits can be more easily discovered using a factor graph.

[47] FIG. 5 is a factor graph representing the parity check matrix of FIG. 4.

[48] A factor graph specifies a parity check matrix. The factor graph is made up of row nodes, column nodes, and connection lines. In FIG. 5, rectangular nodes (upper 4 nodes) indicate the row nodes, round nodes (lower 6 nodes) indicate the column nodes, and lines connecting them to each other indicate the connection lines. The row nodes indicate rows of the parity check matrix, and the column nodes indicate columns of the parity check matrix. When components in locations where the rows and the columns are crossed are 1, the relevant rows and columns are connected to each other by the connection lines. Since a component of the row '1'- column '1' of the parity check matrix in FIG. 4 is 1, row node '1' and column node '1' are connected through the connection line in the factor graph of FIG. 5.

[49] FIG. 6 illustrates a method of selecting correlated code word bits using a factor graph.

[50] A factor graph is used for looking for correlated components in a parity check

matrix. All column nodes connected to each other are correlated in the factor graph. In FIG. 6, column node '1' is connected to column nodes '4' and '6' via row node '1'. Also, the column node '1' is connected to column node '2' via row node '3'. Column nodes '3' and '5' are not connected to the column node '1'. Accordingly, the column nodes '2', '4', and '6' are correlated with the column node '1'.

[51] The number of column nodes in the factor graph indicates the number of code word bits. That is, the column nodes build one row in the parity check matrix by being arranged horizontally, and each component of the row are multiplied by each code word bit in order to generate column parity information.

[52] Accordingly, code word bits having the same number as correlated column nodes are correlated with each other.

[53] FIG. 6 shows that the column node '1' is selected as a first code word bit for generating parity information. As described above, correlated column nodes can be selected using a connection line relationship. First, the column node '1' is connected to column nodes '4' and '6' via a row node '1'. Therefore, the column nodes '1', '4', and '6' are correlated with each other. Also, the column node '1' is connected to a column node '2' via a row node '3'. Therefore, column nodes '1' and '2' are correlated with each other. Putting them together, the column nodes '1', '2', '4', and '6' are correlated with each other. In other words, the code word bits '1', '2', '4', and '6' are correlated with each other. Therefore, if the code word bit '1' is selected for generating the row parity information, it is preferable that the code word bits '2', '4', and '6' not be selected for generating the same parity information P_A . That is, only the code word bits '3' and '5' can be selected for generating the same parity information P_A .

[54] FIG. 7 illustrates a method of selecting a succeeding selectable code word bit when the code word bit '3' is selected as a second code word bit in FIG. 6.

[55] Since the code word bit '3' was selected for generating the parity information P_A , code word bits correlated with the code word bit '3' cannot be selected as a code word bit for generating the parity information P_A any more. Referring to FIG. 7, the column node '3' is connected to column node '5' via row node '4'. Therefore, when a third code word bit is selected, the column node '5' must be excluded.

[56] If the column node '5' is selected as the second code word bit, the code word bit '3' will be excluded since the code word bit '3' is connected to the column node '5' via the row node '4'.

[57] From a fourth code word bit, after unselectable code word bits are excluded using the same method as described above, each code word bit is selected among the residual

code word bits.

[58] To generate the same row parity information, the number of code word bits that must be selected in a code word vector depends on a block size, the number of code word vectors to be used for generating row parity information, and the length of code word vector. If the size of error correction block is 32 Kbytes, the length of code word vector is 1 Kbytes, and the number of code word vectors used for generating row parity information is 16, the number of code word bits to be selected for generating parity information in a code word vector is $32/(1*16) = 2$.

[59] FIGS. 8 through 10 illustrates procedures of selecting residual code word bits when code word bit '2' is selected as a first code word bit in the parity check matrix of FIG. 4.

[60] In FIG. 8, since code word bit '2' was selected as a first code word bit, code word bits '1', '4', and '6' cannot be selected as a second code word bit. Also, if code word bit '3' is selected as the second code word bit as shown in FIG. 9, code word bit '5' cannot be selected as a third code word bit. If the code word bit '5' is selected as the second code word bit as shown in FIG. 10, the code word bit '3' cannot be selected as the third code word bit. Therefore, a selectable code word depends on previously selected code word bits.

[61] In the present invention, a first selection group, a second selection group, ... are defined as selection groups for selecting row code word bits. That is, the first selection group is a set of code word bits that can be selected as the second code word bit determined by selecting the first code word bit, the second selection group is a set of code word bits that can be selected as the third code word bit determined by selecting the second code word bit, and so on.

[62] FIG. 11 is a flowchart of a method of selecting code word bits for generating row parity information using a factor graph.

[63] If a code word vector is determined by generating column parity information, a certain code word bit in the code word vector is selected as a first code word bit. That is, a certain column node in a factor graph is selected as a first selection node in step 1110. A first selection group including only residual nodes except all column nodes connected to the first selection node is generated by checking a structural connection relationship of a factor graph in step 1120. Here, the all column nodes connected to the selection node include all column nodes connected to the selection node via certain row nodes.

[64] A certain column node is selected as a second selection node from the first

selection group in step 1130. Like step 1120, a second selection group including only residual nodes except all column nodes connected to the second selection node is generated in step 1140. Until all selection nodes are determined, steps 1130 and 1140 are repeated from step 1150. If all selection nodes are determined, code word bits corresponding to the selection nodes become code word bits for generating single row parity information in a code word vector in step 1160.

[65] By repeating steps 1110 through 1160 in a second code word vector, code word bits are selected and also used for generating the single row parity information.

[66] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The preferred embodiments should be considered in descriptive sense only and not for purposes of limitation. Therefore, the scope of the invention is defined not by the detailed description of the invention but by the appended claims, and all differences within the scope will be construed as being included in the present invention. 1.

Claims

- [1] 1. An encoding method using a low density parity check (LDPC) matrix, the method comprising:
 generating code word vectors by generating column parity information using a parity check matrix and message information;
 selecting code word bits for generating row parity information among code word bits from which code word bits related to generation of the same row parity information among code word bits in the generated code word vectors are excluded; and
 generating the row parity information using the selected code word bits.
2. The method of claim 1, wherein the selecting of the code word bits is performed on the basis of locations where components of the parity check matrix are 1.
3. The method of claim 1, wherein the selecting of the code word bits comprises: if the first code word bit is related to the generation of the row parity information, and if, in a row number where a component corresponding to the first code word bit in the parity check matrix is 1, a component corresponding to the second code word bit in the row of the parity check matrix is 1, selecting a certain code word bit among residual code word bits except the second code word bit as a code word bit for generating the row parity information.
4. The method of claim 1, wherein the selecting of the code word bits comprises: selecting a certain code word bit of the code word vector as a first selection code word bit;
 generating a first selection group including residual code word bits except code word bits correlated with the first selection code word bit in the code word vector; and
 selecting a certain code word bit among code word bits of the first selection group as a second selection code word bit,
 wherein if the first selection code word bit is related to the generation of row parity information, and if, in a row number where a component corresponding to the first selection code word bit in the parity check matrix is 1, a component corresponding to the second selection code word bit in the row of the parity check matrix is 1, there is a correlation between the first and second selection code word bits.

5. The method of claim 1, wherein the selecting of the code word bits is performed on the basis of a factor graph of the parity check matrix.
6. The method of claim 5, wherein the selecting of the code word bits comprises:
 - generating the factor graph of the parity check matrix;
 - extracting code word bits for generating the same column parity information on the basis of a connection relationship between column nodes included in the factor graph; and
 - selecting a certain code word bit among residual code word bits except the code word bits for generating the same column parity information as a code word bit for generating row parity information.
7. The method of claim 6, wherein the generating of the factor graph comprises:
 - arranging row and column nodes corresponding to row and column numbers of the parity check matrix, respectively; and
 - when components in locations corresponding to the row and column numbers of the parity check matrix are 1, connecting the row and column nodes with connection lines.
8. The method of claim 6, wherein the extracting of the code word bits comprises:
 - selecting a certain code word bit in the code word vector as the first selection code word bit;
 - extracting a first column node corresponding to the first selection code word bit from the factor graph;
 - extracting a certain second column node among residual column nodes except all column nodes connected to the first column node via connection lines; and
 - selecting a code word bit corresponding to the second column node as the second selection code word bit.
9. The method of claim 8, wherein the column nodes connected to the first column node via connection lines comprises all column nodes connected to the first column node via certain row nodes.
10. A method of selecting code word bits used for generating parity information in an information generating operation using an LDPC matrix, the method comprising:
 - selecting a first code word bit; and
 - selecting a second code word bit among residual code word bits except code word bits having a correlation with the first code word bit,
 wherein if the first code word bit is related to the generation of row parity in-

formation, and if, in a row number where a component corresponding to the first code word bit in the parity check matrix is 1, a component corresponding to the second code word bit in the row of the parity check matrix is 1, there is a correlation between the first and second code word bits.

11. The method of claim 10, wherein the correlation is achieved when a column node corresponding to the first code word bit is connected to a column node corresponding to the second code word bit in a factor graph of the parity check matrix.

12. The method of claim 11, wherein the correlation is achieved when the column node corresponding to the second code word bit is connected to the column node corresponding to the first code word bit via a certain row node in the factor graph of the parity check matrix.

Abstract

The present invention relates to a method of independently generating row parity information and column parity information in an encoding process using a low density parity check (LDPC) matrix. The method comprises: generating code word vectors by generating column parity information using a parity check matrix and message information; selecting code word bits for generating row parity information among code word bits in the generated code word vectors; and generating the row parity information using the selected code word bits, wherein the selecting of the code word bits comprises: excluding code word bits related to the generation of other row parity information. Accordingly, independent parity information can be generated by generating row parity information on the basis of code word bits without related to generation of column parity information.

FIG. 1

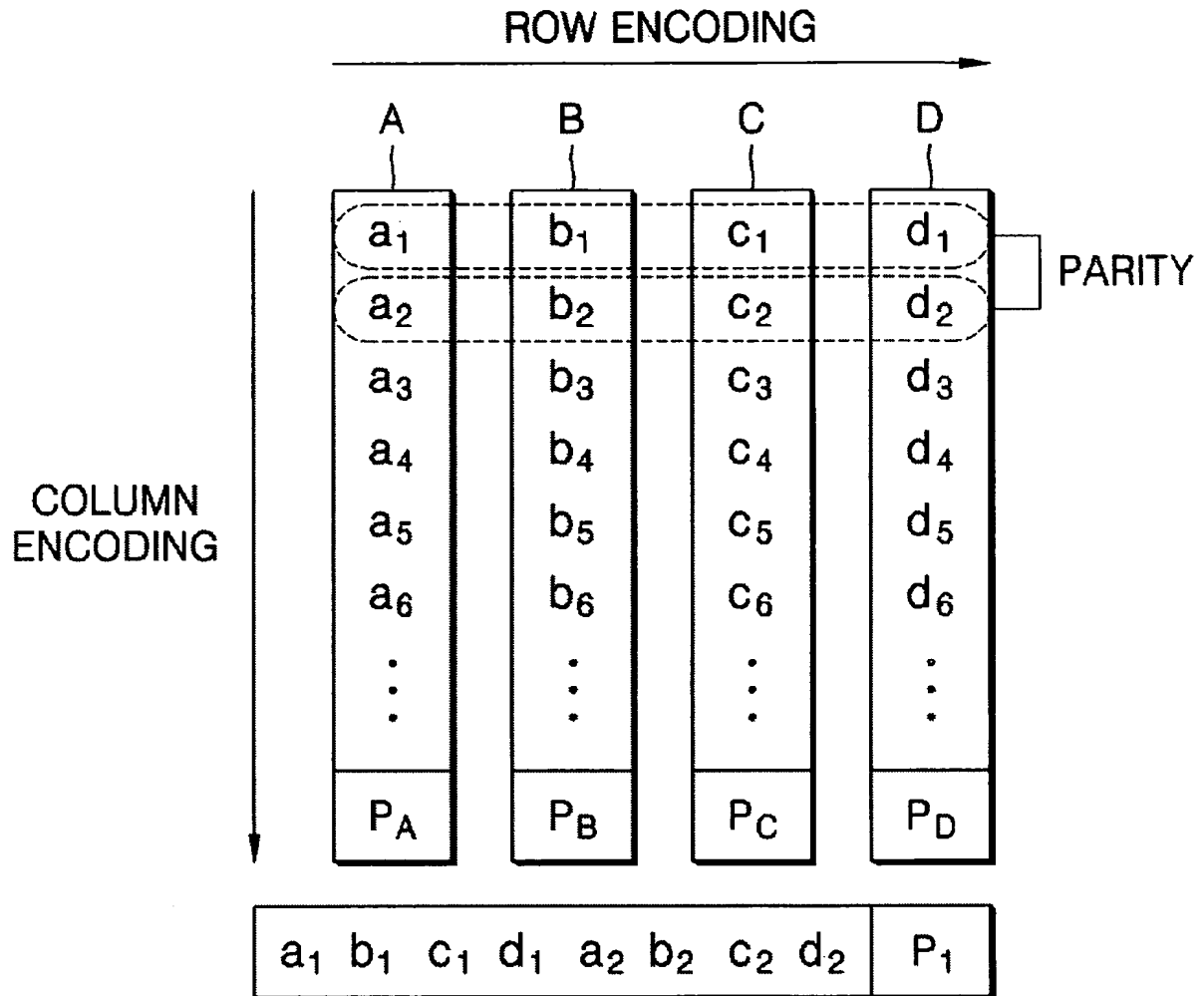


FIG. 2

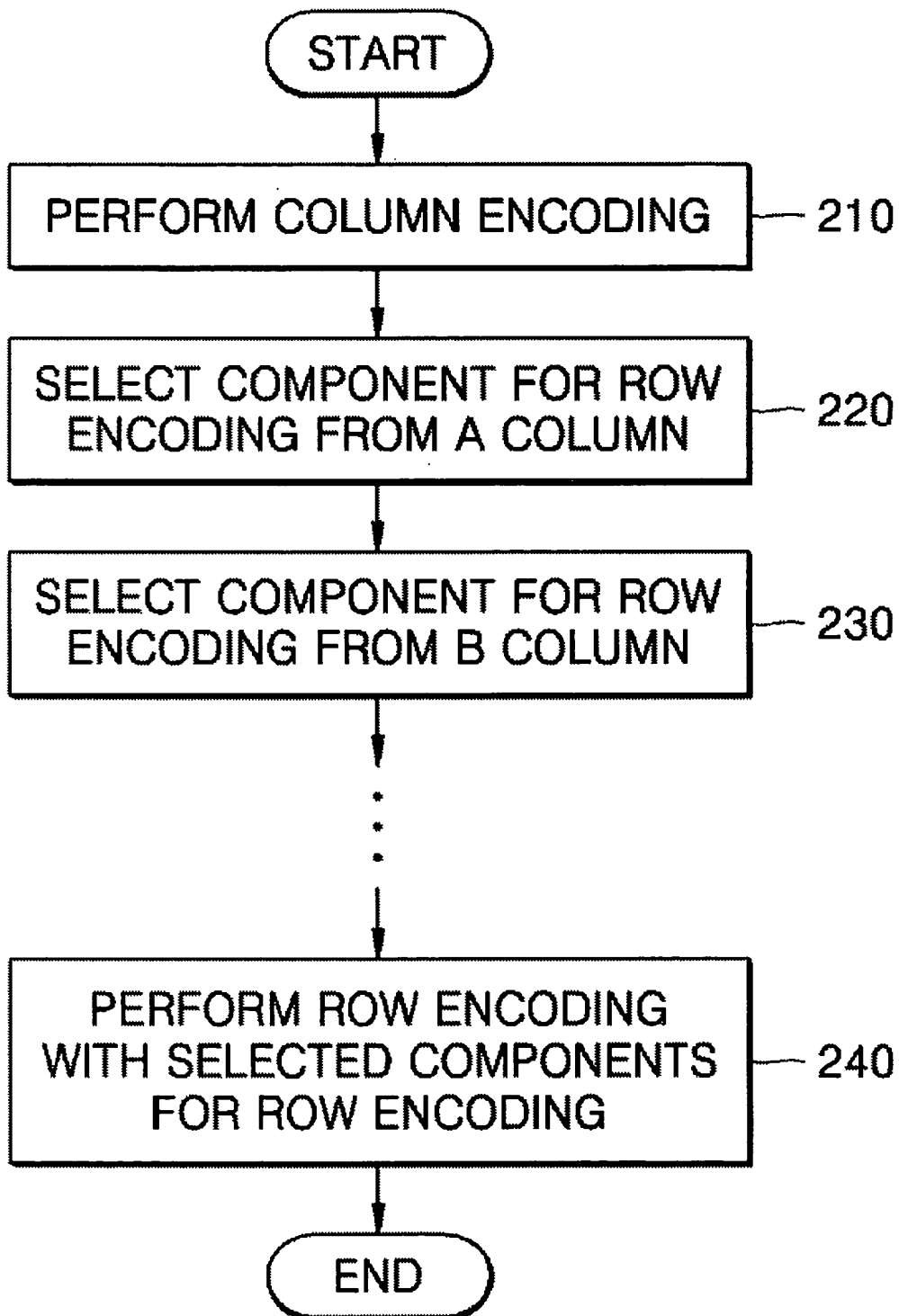


FIG. 3

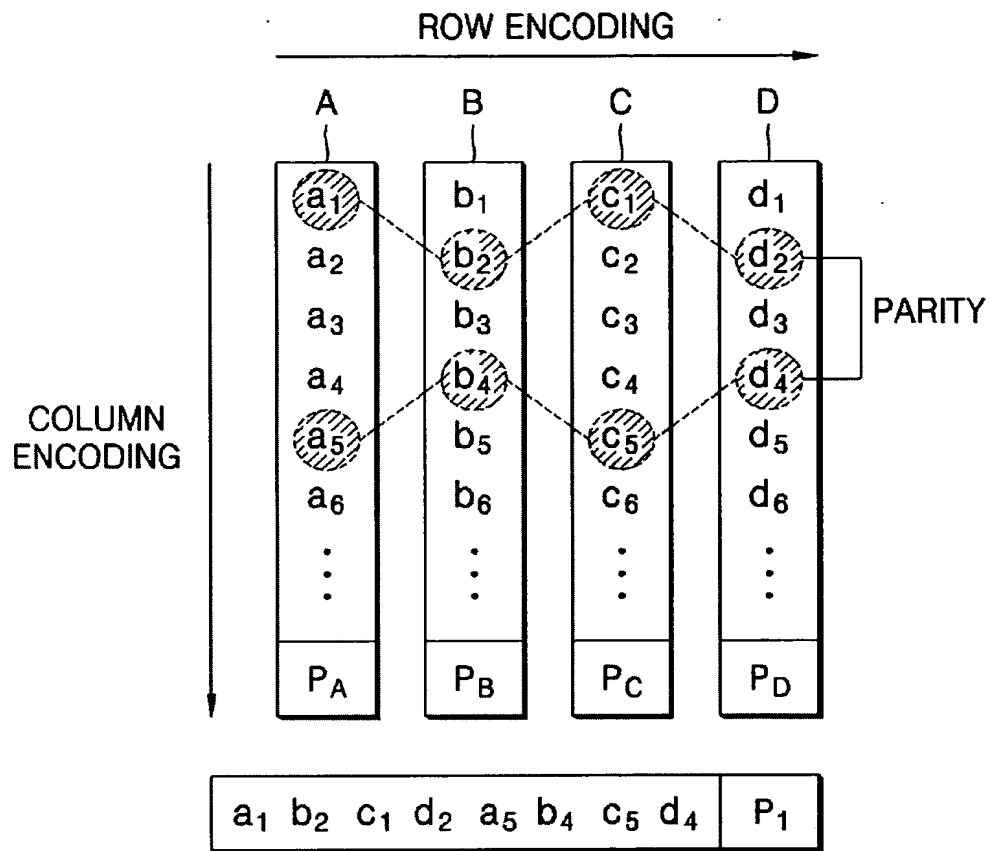


FIG. 4

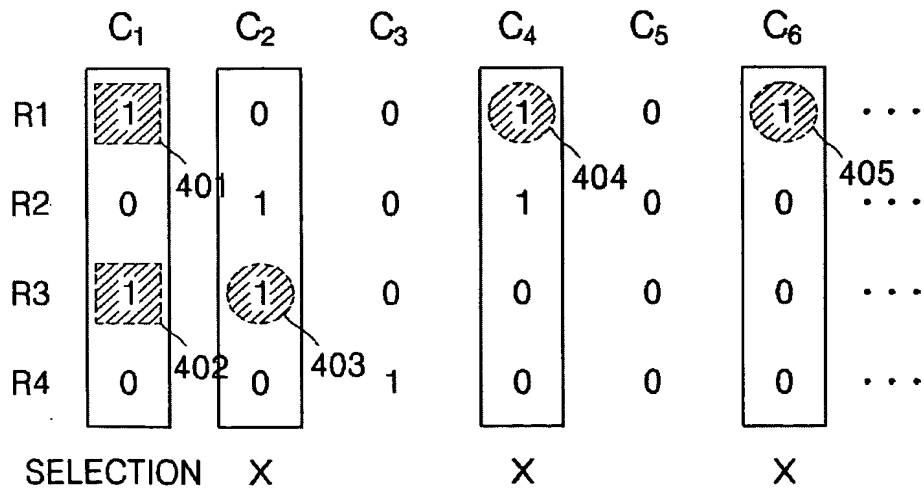


FIG. 5

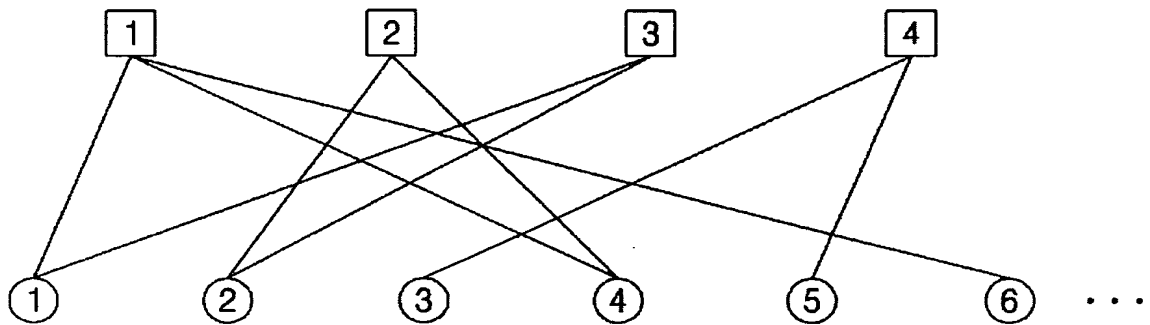


FIG. 6

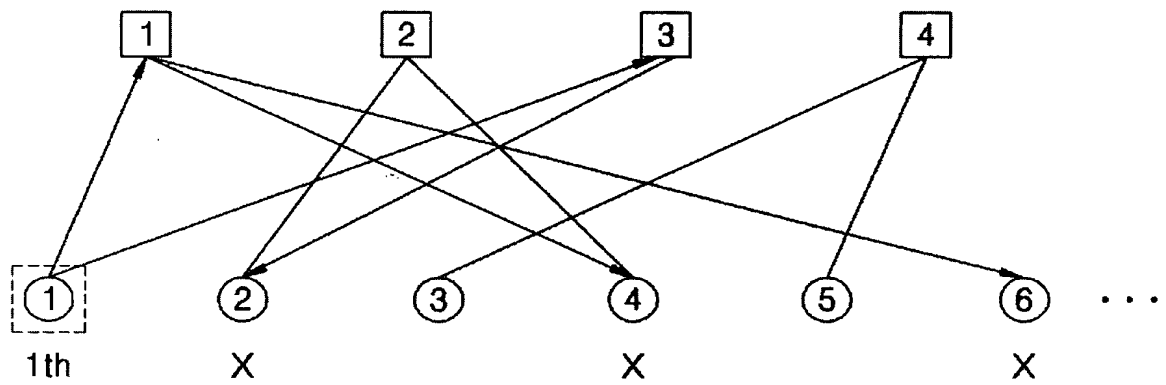


FIG. 7

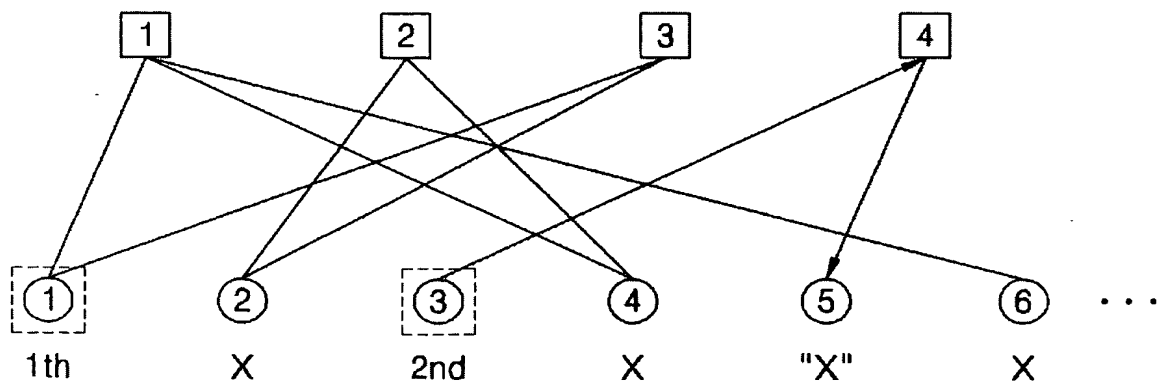


FIG. 8

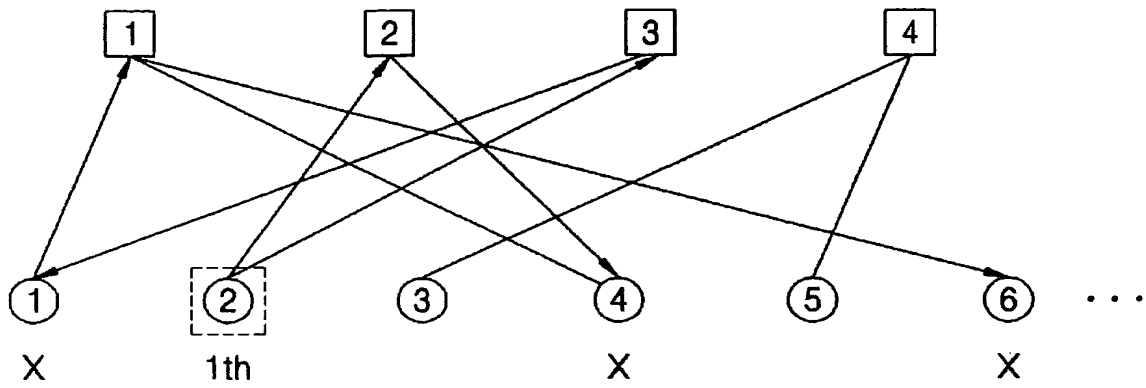


FIG. 9

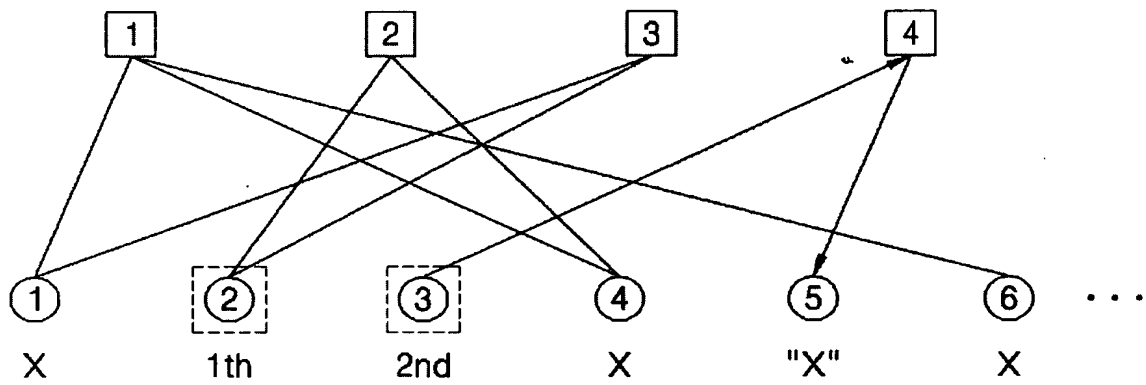


FIG. 10

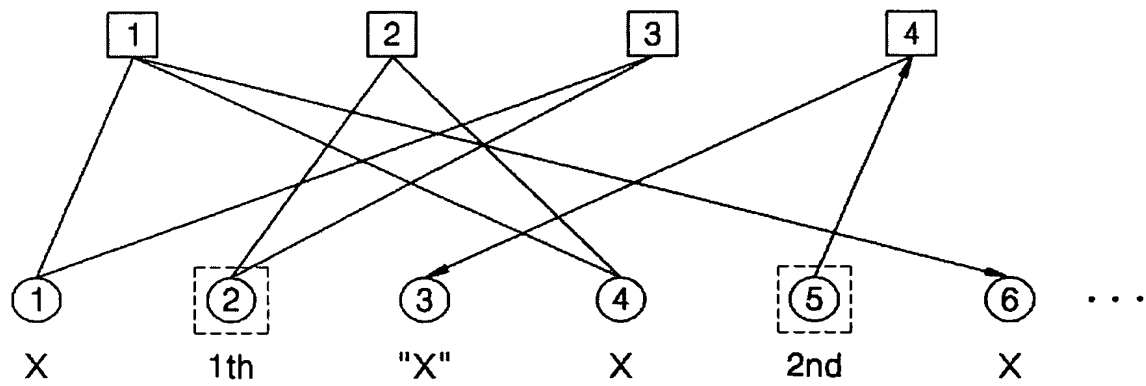


FIG. 11

